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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/041,935	01/07/2002	Yukihisa Kobayashi	9319S-000319	4909
27572	7590	11/28/2006	EXAMINER	
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			ART UNIT	PAPER NUMBER
			3729	

DATE MAILED: 11/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

NT

Office Action Summary

Application No.

10/041,935.

Applicant(s)

KOBAYASHI, YUKIHISA

Examiner

Tim Phan

Art Unit

3729

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 September 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 15, 16, 21-23, 25, 26, 28-32, 37, 38, 40 and 41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 15, 16, 21-23, 25, 26, 28-32, 37, 38, 40 and 41 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The amendment filed on 09/11/06 has been fully considered and made of record.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed language "a band region ... including a second region, a third region ..." (Lines 5 & 6) is indefinite and confused. It is unclear if the band region is the same as the A3 (third) region. The specification and drawings do not provide any clear understanding about the claimed language.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 15, 23, 28-32 and 40 are rejected under 35 U.S.C. 102(e) as being anticipated by Uchiyama (US 6,265,770 B1).

With regard to claim 15, as best understood, Uchiyama teaches a process of mounting a semiconductor component on a substrate (Abstract), comprising:

- solder- mounting first components (Fig. 1, 2; col. 5, lines 20+) within a pair of first regions (Fig. 1, area of 2) on the substrate (Fig. 1, 3);
- forming a band region (Fig. 1, largest surrounding area A) between the pair of first regions including a second region (Fig. 1, A), a third region (Fig. 1, surrounding area A) having wiring patterns (Fig. 1, 10) that join the first components together, and a longitudinal axis or cable axis (Fig. 1, 8) extending from the second region toward the output side terminal (Fig. 1, 12);
- after mounting the first components, arranging an anisotropic conductive film (Fig. 1, 4) within and extending along the longitudinal axis of the band region (Fig. 1, largest surrounding area A) of the substrate;
- arranging a second component (Fig. 1, 6) on the anisotropic conductive film (Fig. 1, 4) such that the anisotropic conductive film is disposed between the second component and the substrate; and
- thermocompression-bonding (Col. 5, lines 56 ff.) the second component (Fig. 1, 6) within

the second region (A) of the substrate.

With regard to claims 23 and 28, Uchiyama teaches that the first component (Fig. 1, 2) is selected from the group of passive and mechanical components (Col. 5, lines 15+), and the second component comprises a semiconductor device (Fig. 1, 6; col. 11, line 37) or LCD or power source IC.

With regard to claim 29, Uchiyama teaches that the band region (Fig. 1, surround of A) can be extended from one end to the other end of the substrate (Fig. 1, 3).

With regard to claim 30, Uchiyama teaches that the band region (Fig. 1, surround of A) extends rectilinearly along the substrate (Fig. 1, 3).

With regard to claim 31, Uchiyama teaches that there are wiring patterns (Fig. 1, 11) on the substrate (Fig. 1, 3) in the band region (Fig. 1, surround of A).

With regard to claim 32, Uchiyama teaches a dummy electrode or ground wire (Fig. 1, 12) at a position associated with the second component or LCD chip (Fig. 1, 6).

With regard to claim 40, Uchiyama teaches that other first components (Fig. 1, right 2) are mounted in another first region (Fig. 1, left 2), the first region (Fig. 1, right 2) and the another

first region disposed on opposing sides of the band region (Fig. 1, surround of A) such that the band region extends between the first regions toward the output side terminal (Fig. 1, 12).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 16, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchiyama (US 6,265,770 B1).

With regard to claim 16, Uchiyama teaches a process of mounting a semiconductor component on a substrate, which reads on applicant's claimed invention, except for mounting the first component (Fig. 1, 2) on the substrate (Fig. 1, 3) by a solder reflow treatment.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to solder (Col. 5, lines 20 ff) the connection by reflow treatment, which is well known in the art, in order to increase production.

With regard to claim 25, Uchiyama teaches the claimed invention, except for providing the alignment marks outside the band region (Fig. 1, largest surrounding area A).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the alignment marks outside the band region since it was known in the art that reference marks are utilized to assign an exact location of the band region (Fig. 1, largest surrounding area A).

With regard to claim 26, Uchiyama teaches that a bonding region by ACF or an outside band region is selected (Fig. 1, areas of 2) where the components are soldered (Col. 5, lines 20+) to the substrate by conventional technique such as solder reflow in order to speed up the soldering process.

8. Claims 21, 22, 37, 38 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchiyama in view of Uchiyama et al (US 5,847,796).

With regard to claim 21, Uchiyama teaches a process of mounting a semiconductor component on a substrate by press-bonding (Abstract), comprising:

- arranging a band region (Fig. 1, surround of A) including a longitudinal axis or cable axis (Fig. 1, 8) extending toward the output side terminal (Fig. 1, 12) of a surface of the circuit board or substrate (Fig. 1, 3) between a pair of first regions (Fig. 1, areas of 2);
- soldering a first component (Fig. 1, 2; Col. 5, lines 20 ff.) onto the circuit board (Fig. 1, 3) outside of the band region (Fig. 1, surround of A); and
- following soldering of the first component (Fig. 1, 2) to the first region (Fig. 1, area of 2), thermocompression-bonding (Col. 5, line 58) a second component (Fig. 1, 6) to the

circuit board within the band region (Fig. 1, surround of A) using an anisotropic conductive film (Fig. 1, 4) under a press-bonding process (Abstract); except for using a compression bonding head where the band region is wider than the head;

Uchiyama et al teach a method of bonding a driver IC (Fig. 3, 1) with a bonding tool or compression bonding head (Fig. 3, 4), slightly wider than the driver IC but much smaller than a band region or upper surface of the substrate (Fig. 3, 62) in order to have a more uniform load at a more uniform temperature of bonding.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the bonding tool or compression bonding head, as taught by Uchiyama et al, to the IC mounting process of Uchiyama, in order to have a more uniform load at a more uniform temperature of bonding.

With regard to claim 22, Uchiyama et al in view of Uchiyama teach the claimed invention, including the thermal press-bonding (Uchiyama, Col. 5, lines 57+) and a heated bonding head or bonding tool (Uchiyama et al, Fig. 10, 4) pressing against the component (Uchiyama et al, Fig. 10, 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a heated bonding head pressing against the component (Uchiyama et al, Fig. 10, 1) in selected area (Uchiyama, Fig. 1, area of A) without hitting the first component (Uchiyama, Fig. 1, 2) in order to concentrate all the heat toward melting the anisotropic conductive film (Uchiyama, Fig. 1, 4) under the chip (Uchiyama, Fig. 1, 6).

With regard to claim 37, Uchiyama teaches that the band region (Fig. 1, surround of A) is narrower than a surface of the circuit board or substrate (Fig. 1, 3).

With regard to claim 38, Uchiyama teaches that other components (Fig. 1, left 2) are mounted in another region located outside of the band region (Fig. 1, A) is disposed on the surface of the circuit board (Fig. 1, 3) on a side of the circuit board that opposed the first regions (Fig. 1, right 2).

With regard to claim 41, Uchiyama teaches a process of mounting a semiconductor component on a substrate by press-bonding (Abstract) including the bonding of the second component (Fig. 1, 6) between the first components (Fig. 1, 2), which reads on applicants' claimed invention.

Uchiyama et al teach a method of bonding a driver IC (Fig. 3, 1) with a bonding tool or compression bonding head (Fig. 3, 4), slightly wider than the driver IC but much smaller than a band region or upper surface of the substrate (Fig. 3, 62) in order to have a more uniform load at a more uniform temperature of bonding.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the bonding tool or compression bonding head, as taught by Uchiyama et al, to the IC mounting process of Uchiyama, in order to have a more uniform load at a more uniform temperature of bonding.

Response to Arguments

9. Applicant's arguments with respect to claims 15, 16, 21-23, 25, 26, 28-32, 37, 38, 40 and 41 have been considered but are moot in view of the new grounds of rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.


Art Unit: 3729

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim Phan whose telephone number is 571-272-4568. The examiner can normally be reached on M - F, 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tim Phan
Examiner
Art Unit 3729



A. DEXTER TUGBANG
PRIMARY EXAMINER

tp
November 21, 2006